WHAT IS CLAIMED IS:

Sub B6

1. A method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said dummy trenches and said wide and narrow trenches with a conductive material;

polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said narrow and wide trenches, wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.

Sub B7

2. The method of claim 1, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. The method of claim 1, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.

6. The method of claim 5, wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.

Sub C2

7. The method of claim 5, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

Sub A6

9. A method for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive a relatively narrow interconnect feature;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors bounded exclusively within said dummy trenches electrically separate from said electrically conductive features, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features.

Sub B3

10. The method of claim 9, wherein said conductive material comprises a metal selected from said group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said wide and narrow trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. The method of claim 9, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to said upper surface.

14. The method of claim 13, wherein said polishing further comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said upper surface of said conductive material.

15. The method of claim 13, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. The method of claim 9, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

Sub A7

17. A substantially planar semiconductor topography elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit, comprising:

a plurality of laterally spaced dummy trenches residing within a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors bounded exclusively within said dummy trenches and electrically separate from said plurality of electrically conductive features; and

interconnect bounded exclusively within said narrow and wide trenches, wherein interconnect upper surfaces are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

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